Code No. : 21114

VASAVI COLLEGE OF ENGINEERING *(Autonomous)*, HYDERABAD

B.E. (C.S.E.) II Year I-Semester (Main) Examinations, Nov./Dec.-2016

Computer Architecture

Time: 3 hours Max. Marks: 70

*Note: Answer **ALL** questions in **Part-A** and any **FIVE** from **Part-B***

Part-A (10 × 2 = 20 Marks)

1. What are the micro operations that can be used to selective-set bits of register?
2. A register R=11011101, determine the sequence of binary values in *R*after a logical shift-left, followed by a circular shift-right, followed by a logical shift-right and a circular shift-left.
3. List the various registers of a basic computer.
4. The control memory has 4096 words of 24 bits each. How many bits are there in the control address register?
5. What is the difference between logical and arithmetic shift operations?
6. Determine the number of clock cycles that it takes to process 200 tasks in a six-segment pipeline.
7. Outline the concept of programmed I/O.
8. Show how the zero insertion works in the bit-oriented protocol when a zero followed by the 10 bits that represent the binary equivalent of 1023 are transmitted.
9. Define Bootstrap loader.
10. A digital computer has a memory unit of 64K X 16 and a cache memory of 1K words. The cache uses direct mapping with a block size of four words. How many bits are there in the tag, index, block, and word fields of the address format.

Part-B (5 × 10 = 50 Marks)
(All bits carry equal marks)

11. a) Describe Bus Interconnection.

    b) Register A holds the 8-bit binary 11011001. Determine the *B* operand and the logic microoperation to be performed in order to change the value in *A* to:

    i. 01101101

    ii. 11111101

12. a) Design a common bus system to interconnect basic computer registers with memory unit.

    b) Derive the control gates associated with the Address Register (AR) in the basic computer with neat diagram.

13. a) Design hardware for addition and subtraction using signed-magnitude data.

    b) Explain four possible hardware schemes that can be used in an instruction pipeline in order to minimize the performance degradation caused by instruction branching.

14. a) Explain how priority interrupt hardware assigns priorities when more than two interrupts occur.

    b) In most computers an interrupt is recognized only after the execution of the instruction. Consider the possibility of acknowledging the interrupt at any time during the execution of the instruction. Discuss the difficulty that may arise.

Contd... 2

Code No. : 21114

15. a) Explain main memory connection to the processor with a neat diagram.

    b) A virtual memory has a page size of 1K words. There are eight pages and four blocks. The associative memory page table contains the following entries:

Page	Block
0	3
1	1
4	2
6	0

    Make a list of all virtual addresses (in decimal) that will cause a page fault if used by the CPU.

16. a) Design a 4-bit combinational circuit decrementer using four full-adder circuits.

    b) Illustrate micro programmed control organization.

17. Answer any ***two*** of the following:

    a) Explain stack organization.

    b) Distinguish Synchronous and Asynchronous Data transfer.

    c) Discuss memory management hardware.

****